Distributed Instruction Queue for Low-Power Microprocessors

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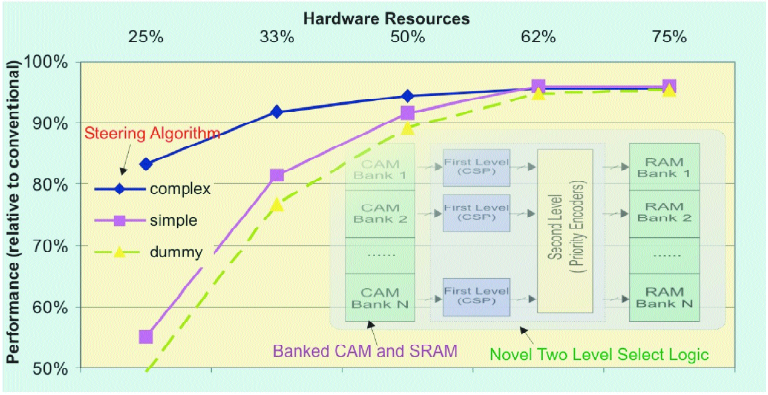

The proliferation of wireless and portable systems and the growing field of sensor networks have heightened the demand for energy-efficient microprocessors. In a superscalar microprocessor, the instruction queue (IQ) is a very energy-inefficient unit consisting of a CAM, select logic, and an SRAM. A distributed IQ has been developed to enable a tradeoff between performance and power consumption through allocation of hardware resources. The distributed IQ introduces an additional instruction-steering stage to improve hardware utilization and achieve higher energy efficiency. Simulations on SPEC 2000 benchmarks show that, with a simple steering algorithm, a distributed IQ with 75% hardware resources can achieve 96% IPC performance compared to the conventional IQ and can still achieve 55% performance with as little as 25% hardware resources. To further improve the IQ, a two-level select logic unit has been implemented. In the first level, cyclic segmented prefix (CSP) circuits implement an oldest-first selection policy, and final select arbitration is achieved by a simple position-based circuit in the second level. With dynamic logic implementation, the two-level select logic reduces delay by 32% compared to the conventional approach.