A Dynamic Reconfigurable A/D Converter for Sensor Applications

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There is tremendous value to dynamically controlling the resolution and speed of A/D conversion in many sensor systems due to variable sensor characteristics, desire to quickly scan arrays before measuring a specific element with high resolution, and the opportunity to minimize power consumption during extended periods of inconsequential data. A hybrid algorithmic-ΣΔ A/D converter has been developed wherein the residual of a ΣΔ conversion is iteratively fed back and resampled to embed bit-weight information into the digital output sequence, as performed in an algorithmic conversion using the extended counting technique. By varying the number of sampling and feedback cycles, the ADC is capable of dynamic self-adjustment between a more ΣΔ-like architecture (with higher resolution and slower speed) and a more algorithmic-like architecture (with faster speed and lower resolution). For a nominal clocking frequency of 10MHz, the ADC can resolve 8 bits in 1.6μsec, 16 bits in 51.2μsec, or various configurations in between (see Operational Space plot). The hybrid algorithmic-ΣΔ A/D converter has been implemented in 0.5μm CMOS and occupies less than 0.4mm^2. This ADC can significantly improve the performance characteristics of low power integrated microsystems such as those being developed within the WIMS ERC.