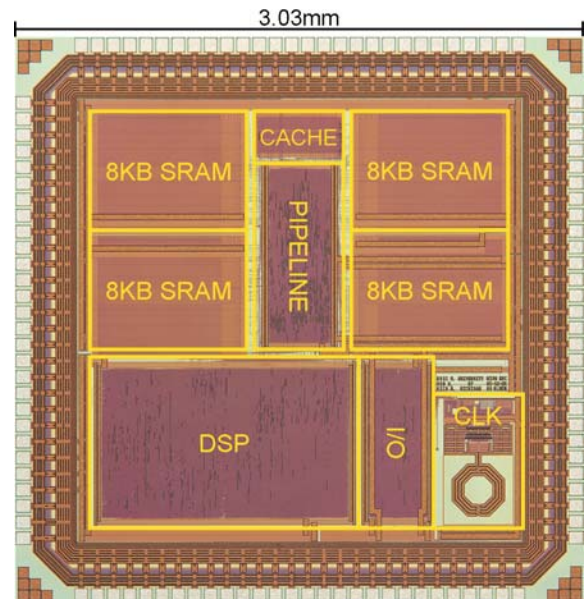


## A DSP Capable Microsystem for Use in Cochlear Implants

Eric Marsman, Robert Senger, and Richard B. Brown

The next-generation WIMS Microcontroller has been realized in a TSMC 0.18 $\mu\text{m}$  process, occupies 9.18mm<sup>2</sup>, and contains 2.3 million transistors. This is a 28% reduction in area over the previous version. It combines an energy-efficient microcontroller unit (MCU), a low-power DSP core, and a monolithic self-referenced hybrid temperature-compensated LC oscillator (TC-LCO) and ring oscillator clock reference in a single bulk CMOS SoC. The 16-bit MCU contains a 3-stage pipeline, 32kB of on-chip memory, a loop cache, and several peripheral communication interfaces. The DSP core performs a 16-channel version of the Continuous Interleaved Sampling (CIS) speech processing algorithm. The low-power architecture is expandable, programmable, and fully-synthesizeable. Interfaces to an external ADC and electrode array are included. The self-referenced hybrid clock source, courtesy of Mobius Microsystems, consists of a highly-accurate TC-LCO and an independent tunable ring oscillator. The synthesizer supports a reduced-power standby mode in which the TC-LCO is powered down while the system operates from the low-power, low-frequency ring oscillator. The entire clock synthesizer occupies 0.25mm<sup>2</sup> of silicon area. Maximum power consumption of the complete microsystem is 45.64mW at 100MHz and 1.8V. On-the-fly frequency scaling allows an operating range of 78kHz to 100MHz. Operating at 10MHz and 1.2V reduces the complete microsystem power consumption to 2.54mW. DSP mode consumes 1.79mW from a 1.2V supply, the lowest reported digital CI power consumption. Standby power consumption is 370 $\mu\text{W}$ , a 50% reduction over the previous microsystem.



**Die micrograph of the complete microsystem in the TSMC 0.18 $\mu\text{m}$  mixed-mode RF process.**