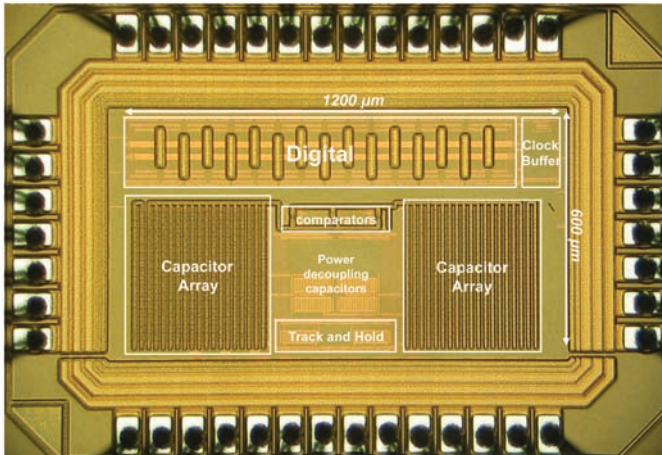


## A 12b, 11MS/s Successive Approximation ADC With Two Comparators in 0.13 $\mu$ m CMOS

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The SAR analog-to-digital conversion architecture is popular because of its energy efficiency; however, the SAR architecture is less used for resolutions above 10b. A two-comparator architecture, incorporating deliberate comparator offset and pre-amplifier power management, reduces comparator metastability and comparator power consumption in a 12b 11MS/s SAR ADC. A prototype, fabricated in 0.13 $\mu$ m CMOS achieves an FOM of 31fJ/conversion step, an SNDR of 62.4dB, an SFDR of 72.8dB, and an error rate of  $<1.9 \times 10^{-12}$  at 11MS/s. ■

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