

A Digital Fractional-N Frequency Synthesizer With Improved Data Rate and Energy Efficiency

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A fractional-N frequency synthesizer is a key building block of wireless systems because it can both generate a high-frequency signal with a well-defined frequency and modulate that signal, allowing an entirely wireless transmitter to be implemented with only a fractional-N frequency synthesizer and a power amplifier. Two limitations of this architecture have been overcome: the reliance on complex analog circuitry in deep sub-micron technology, and the trade-off between low-loop bandwidth for good $\Sigma\Delta$ noise rejection and high-loop bandwidth for fast modulation rates. First, new techniques make the design more straightforward by eliminating analog circuitry, which in turn improves energy efficiency by allowing signal processing to be done digitally in nanometer complementary metal oxide semiconductor (CMOS) technology. Specifically, the new architecture uses a novel all-digital phase detector in place of the conventional analog-intensive phase detector, charge pump, and loop filter blocks. Second, a digital dual-modulation scheme is used to alleviate the tradeoff between loop bandwidth and modulation rates. A 14mW, 2.2GHz minimum shift keying (MSK) transmitter with a transmission rate of 927.5kbit/s has been demonstrated. Energy efficiency is improved by a factor of 3 compared to the state-of-the-art. ■

